ARCS Model

Course Name: Computer Architecture & Organization

Topic: Pipeline Architecture **Academic Year:** 2016 -17

Class/Section: IV ECE B **Semester:** I

Learning objective for the lecture: The student can:

- ✓ Examine pipeline architecture processor - RISC Pipeline Vector processing.

Component	**Implementation Strategies**
Attention (What is interesting about this?) ***Topic Content*:** Pipeline Architecture - RISC processor	To draw the learners **Attention:** 1. Started class with brainstorming session by posing questions on what is meant by pipeline, multitasking, parallel execution, task breaking, etc., 2. Since pipeline architecture is an advanced technology, proposed to arrange 'Summer Internship' to Defense Research Organization. 3. Gave real live product car fabrication which is fabricated in a pipelined fashion. 4. To understand the real concept of throughput calculation video lectures is played with animation drawn from NPTEL courses. 5. Used a variety of methods to reinforce the course material and which helps to incorporate a variety of learning styles.
Relevance (Why should I be wasting my time studying this?) ***Topic Content*:** Pipeline Architecture - RISC processor	My strategies to accomplish the **Relevance:** 1. The importance of new leavening was briefed to the students. This concept is more useful for microprocessor based embedded systems for which lot of avenues are open; also useful to get jobs in IoT related applications. A lot of demand in FABS companies, Chip fabrication companies, for students who are strong in Pipeline Architecture 2. Case studies: some case studies have given related to RISC, CISC Processor based computers mostly used in weather forecasting. 3. Goal oriented students: For those students who dream of pursuing higher studies and do research this is one area where there is a lot of scope. 4. Machine Learning applications (especially Artificial Neural Networks) executing speed plays a major role so using pipe line architecture processor speed can be enhanced. 5. Role Model: One super senior of our college presently who is working for INTEL company after finishing his MS in US, doing the job of ***writing microprogramming*** code for dual processors.

Confidence (This is not Difficult-I can do it) ***Topic Content***: Pipeline Architecture - RISC processor	To build a sense of **Confidence in** learners: 1. **Motivation:** At the beginning of the semester, the students were told about the evaluation process. The importance of each examination including online exam and home assignments is very much motivated. The students will be motivated with quotes like ' if the first button of a shirt is put wrongly, rest of the buttons also will be put wrongly, in the same if a student fails in one semester its impact will be there on rest of the semesters. 2. **Self-Growth:** Each student was asked to prepare their future Goals, type neatly display in his/her study room. They were also asked to display great scientist's photos like Einstein, Faraday, in the study room. The Goals are revised by me frequently. They are also advised to participate in Campus Recruitment Training Courses and technical workshops. Goals are verified by T&P faculty once in a month and were asked to rewrite/modified their own Goals. 3. **Feedback:** Mentors are appointed for every 20 students to monitor their performance in every month. Mid exam marks are displayed on notice board and poor performance students are motivated to improve their performance. Slow learners are identified based on their performance; special care is taken for such students to improve their performance. 4. **Small Group Activities**: The learners are divided into groups of three to six. Each group is assigned a team number and each group member is assigned a unique id. When the trainer poses a question, group members get together, examine the possibilities, and construct an answer. The trainer then picks a number by drawing a card or rolling a die. The number selected designates the spokesperson for each table group. A second number designates the table group that will respond first. By involving in such group activities students are well motivated.
Satisfaction (This is great - I have learned something new and useful) ***Topic Content*:** Pipeline Architecture - RISC processor	**Learner's Satisfaction:** 1. Outstanding performance students are appreciated through rewards in public, like their names are displayed in college notice board, special appreciation letter from the principal, fee wavering from management. 2. Parents whose wards are selected on-campus drives are felicitated along with their ward on Graduation Day. It gives motivation to juniors and self satisfaction for selected students. 3. Equity: Transparency is maintained in all evaluation systems. Perfect rubrics are defined and displayed for students. The examination system is transparent and all mid marks are displayed in notice boards.

Implementation of Strategies

Significance of results & reflective critique:

The objective of this assignment is to learn how to apply the ARCS model to the content that is teaching. The concept says students learn best

i) When the teacher can generate sufficient interest in the topic being studied,

ii) When the content is relevant,

iii) One might feel they can master it, and

iv) When they have the feeling that their effort has been well rewarded and they have learned something new and useful.

Video Link:
https://www.youtube.com/watch?v=3p8kZpT56lQ
Course Materials:

Teams and Evaluation:

Regd. No	Name of the Student	Team ID	TEAM	1st Round	2nd Round	3rd Round
13NM1A0453	KOMATINENI SINDU SREE	A1(L)	A	5M	0M	
13NM1A0454	KOTA MANISHA	A2				
13NM1A0455	KOTRA SANDHYARANI	A3				
13NM1A0456	KUCHIPUDI SOWJANYA	A4				
13NM1A0457	KUNDRAPU YAMINI	A5				
13NM1A0458	KURADA GANGA BHAVANI	B1(L)	B	5M	5M	0M
13NM1A0459	LALAM VARALAKSHMI	B2				
13NM1A0462	MADAKASSERIYIL BINDHU	B3				
13NM1A0463	MADDALA HEMALATHA	B4				
13NM1A0464	MADDI ASRITHA	B5				
13NM1A0465	MAKENA LALITHA MADHURI	C1(L)	C	0M		
13NM1A0466	MANASA PENUMATSA	C2				
13NM1A0467	MANCHIRAJU SIRISHA KAMESWARIDEVI	C3				
13NM1A0468	MANDALA LALITHA	C4				
13NM1A0469	MANDALA RAMANI	C5				
13NM1A0470	MARPU SUSHMA	D1(L)	D	5M	0M	
13NM1A0471	MATTE HARIKA	D2				
13NM1A0472	MATTHURTHI VENKATA PAVANI	D3				
13NM1A0473	MEDAPATI SUBHASHREE	D4				
13NM1A0474	MUMMANA BHAVANI	D5				

13NM1A0475	MUNAGAPAKA LAKSHMI	E1(L)	E	0M		
13NM1A0476	MUNI VENKATA ANJALI UMAMAHESWARI	E2				
13NM1A0477	MUSUNOORI ANU PRIYANKA	E3				
13NM1A0478	NALLAM LAKSHMI BHAVANI SHIVA SHRUTHI	E4				
13NM1A0479	NANEPALLI VASANTHI	E5				
13NM1A0480	PAILA BHAVANI	F1(L)	F	5M	5M	0M
13NM1A0481	PASALA BHAVANI	F2				
13NM1A0482	PASUMARTHI PRATHYUSHA	F3				
13NM1A0483	PATIVADA MAMATHASRI	F4				
13NM1A0484	PEDDI HASINI	F5				
13NM1A0485	PENKE BHARATHI	G1(L)	G	5M	5M	5M
13NM1A0486	PENTAPATI SWETHA	G2				
13NM1A0487	PILLA CHAMUNDI RAMA	G3				
13NM1A0488	PILLA T S SAILAJA	G4				
13NM1A0489	PINNAMARAJU S S TEJASWINI	G5				
13NM1A0490	POLAMARASETTY DIVYA	H1(L)	H	5M	0M	
13NM1A0491	RAJANA SANDHYA	H2				
13NM1A0492	RAVADA NAVYA NIRMALA	H3				
13NM1A0493	RAVALLA SOWJANYA	H4				
13NM1A0494	RAYEEBONU HARITHA	H5				
13NM1A0495	REESU SHYAMALA VENKATA LAXMI	I1(L)	I	5M	5M	
13NM1A0496	REGULAGEDDA SAI ADBUTHA	I2				
13NM1A0498	RONGALI RENUKA	I3				
13NM1A0499	S GAUTAMI	I4				
13NM1A04A0	S HARSHITHA	I5				
13NM1A04A1	SALAPU SUKANYA	J1(L)	J	5M	0M	
13NM1A04A2	SARAGADAM BHAGYASREE	J1				
13NM1A04A3	SEELAM LATHA SREE	J3				
13NM1A04A4	SESHAPU DURGA BHAVANI	J4				
13NM1A04A5	SETTI TEJASWI	J5				

Questions:

1. Define Pipeline processing.
2. What is Pipelining?
3. What are the major characteristics of a Pipeline?
4. What are the various stages in a Pipeline execution?
5. What are the types of pipeline hazards?

6. What is instruction level parallelism?
7. Draw the hardware organization of two stage pipeline.
8. List the various pipelined processors.
9. Why we need an instruction buffer in a pipelined CPU?
10. What are the problems faced in instruction pipeline?

Best performance Team:

13NM1A0485	PENKE BHARATHI	G1(L)	15M
13NM1A0486	PENTAPATI SWETHA	G2	
13NM1A0487	PILLA CHAMUNDI RAMA	G3	
13NM1A0488	PILLA T S SAILAJA	G4	
13NM1A0489	PINNAMARAJU S S TEJASWINI	G5	

Activity Outcome-PO Mapping:

Activity Outcome	Mapping to PO's
Compare RISC and CISC Architectures	**PO3,PO7, PO10,PO12**
Justify the merits of Pipeline processing	**PO1,PO9**

Post Implications:

- Students actively participated in the activity
- Communication skills are improved
- Team work together improves their performance